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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/730,195	12/05/2000	Eric J. Helmsen	FORE-76	7958

7590

06/07/2004

Ansel M. Schwartz  
201 N. Craig Street, Suite 304  
Pittsburgh, PA 15213

EXAMINER

MEEK, JACOB M

ART UNIT	PAPER NUMBER
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2631

DATE MAILED: 06/07/2004

4

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/730,195

Applicant(s)

HELMSEN ET AL.

Examiner

Jacob Meek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 12/05/2000.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1 - 26 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-9, 14, 15, 16 - 18, 25, 26 is/are rejected.
- 7) ☒ Claim(s) 10-13, 19 - 23 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
  - ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Claim Objections***

1. Claims 11, 12 are objected to because of the following informalities: correct spelling of "comparator". Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 14 and 24 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. In particular, Claims 14 and 24 state, "which are outside of a predetermined acceptable range." This "predetermined acceptable range" appears to be critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 15 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular Claim 15, "predetermined acceptable range is \_\_\_\_\_" does not clearly state a limitation.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1 - 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Urbansky in view of Goto.

Urbansky teaches a timing distribution system consisting of a signal source and a first filter (see Figures 1 & 2) for the removal of jitter and wander (claim 1). Urbansky does not explicitly teach a second filter, but he does state there may be a requirement for such a filter (page 535, paragraph below Figure 1). Goto teaches timing system comprised of a signal source, a first filter, and a second filter (See Figure 2). Goto teaches the need for a first loop with high enough bandwidth and gain to pull-in signals quickly to accommodate jitter and rapid phase transients, and a second loop with low enough bandwidth and gain to maintain clock stability in holdover mode (to accommodate wander and meet MTIE requirements, column 1, lines 46 – 64). It would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt Urbansky's device to provide jitter (1<sup>st</sup> filter, high bandwidth) and wander (2<sup>nd</sup> filter, low bandwidth) filters since Goto teaches that his invention addresses the limitations of conventional PLLs which are unable to achieve both short pull-in times and stable holdover operation (see Column 1, lines 34 –36).

5. Urbansky teaches the first filter includes a first tuneable directed digital synthesizer connected to the source for producing a clock signal derived from the signal from the source (Claim 2) (see Figure 2, Numerically Controlled Oscillator block).
6. Urbansky teaches the source includes an oscillator that produces the signal (Claim 3) (See Figure 2, Numerically Controlled Oscillator block).
7. Urbansky teaches the first filter includes a reference input clock signal mechanism for providing a reference input clock signal with respect to the clock signal (Claim 4) (See Figure 2, see Digital Phase Detector block).
8. Urbansky teaches the first comparison mechanism (claim 5), and discusses the possibility of implementing this function using a microprocessor or with hardware (claim 6) (See page 535, section II, last paragraph).
9. Urbansky does not explicitly teach the second filter includes a second tuneable directed digital synthesizer connected to the first filter for producing a second clock signal from the first clock signal from the first filter a second filter, but he does state there may be a requirement for such a filter (Claim 7) (page 535, Section II, fourth paragraph). Goto teaches timing system compromised of a signal source, a first filter, and a second filter (See Figure 2). Goto teaches the need for a second loop with low enough bandwidth and gain to maintain clock stability in holdover mode (relates to MTIE and wander requirements, column 1, lines 46 – 64). It would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt Urbansky's device to include a wander (2<sup>nd</sup> filter, low bandwidth) filter since Goto teaches that his

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invention addresses the limitations of conventional PLLs which are unable to achieve both short pull-in times and stable holdover operation (see Column 1, lines 34 –36).

10. Urbansky does not explicitly teach the second filter includes a second comparison mechanism which accumulates error between the first clock signal and the second clock signal and produces a second error correction signal to tune the second directed digital synthesizer, but he does state there may be a requirement for such a filter (Claim 8) (Page 535, Section II, fourth paragraph). Goto teaches timing system compromised of a signal source, a first filter, and a second filter (See Figure 2). Goto teaches the need for a second loop with low enough bandwidth and gain to maintain clock stability in holdover mode (relates to MTIE and wander, column 1, lines 46 – 64). It would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt Urbansky's device to include a wander (2<sup>nd</sup> filter, low bandwidth) filter since Goto teaches that his invention addresses the limitations of conventional PLLs which are unable to achieve both short pull-in times and stable holdover operation (see Column 1, lines 34 –36).

11. Urbansky does not explicitly teach the first filter removes noise greater than 1 KHz from the signal and the second filter removes noise less than 1 KHz from the signal, but he does state there may be a requirement for such an arrangement (Claim 9) (page 535, Section II, fourth paragraph). Goto teaches timing system compromised of a signal source, a first filter, and a second filter (See Figure 2). Goto teaches timing system compromised of a signal source, a first filter, and a second filter (See Figure 2). Goto teaches the need for a first loop with high enough bandwidth and gain to pull-in

signals quickly to accommodate jitter and rapid phase transients, and a second loop with low enough bandwidth and gain to maintain clock stability in holdover mode (to accommodate wander and meet MTIE requirements, column 1, lines 46 – 64). Goto does not state the cutoff frequencies of his filters but these would be a design choice. It would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt Urbansky's device to provide jitter (1<sup>st</sup> filter, high bandwidth) and wander (2<sup>nd</sup> filter, low bandwidth) filters since Goto teaches that his invention addresses the limitations of conventional PLLs which are unable to achieve both short pull-in times and stable holdover operation (see Column 1, lines 34 –36).

12. Claims 16 - 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Urbansky in view of Goto.

Urbansky teaches a timing distribution system consisting of a filter (see Figures 1 and 2) for the removal of jitter and wander (claim 16). Urbansky does not explicitly teach a second filter, but he does state there may be a requirement for such a filter (page 535, paragraph below Figure 1). Goto teaches timing system comprised of a signal source, a first filter, and a second filter (See Figure 2). Goto teaches the need for a first loop with high enough bandwidth and gain to pull-in signals quickly to accommodate jitter and rapid phase transients, and a second loop with low enough bandwidth and gain to maintain clock stability in holdover mode (to accommodate wander and meet MTIE requirements, column 1, lines 46 – 64). It would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt Urbansky's device to provide jitter (1<sup>st</sup> filter, high bandwidth) and wander (2<sup>nd</sup>

filter, low bandwidth) filters since Goto teaches that his invention addresses the limitations of conventional PLLs which are unable to achieve both short pull-in times and stable holdover operation (see Column 1, lines 34 –36).

13. Urbansky teaches the removing the jitter step includes the step of applying an error correction signal to a direct digital synthesizer of the first filter by a first microcontroller of the first filter based on accumulated error between a reference input clock signal and a clock signal from the direct digital synthesizer (claim 17)(see Figure 2).

14. Urbansky teaches that before the removing the jitter step, there is the step of producing the clock signal from the signal from an oscillator (claim 18) (See Figure 2).

15. Claims 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Bertacchini in view of Bedrosian.

Bertacchini teaches a means for monitoring and protection switching a failed clock reference that is phase aligned with other reference clocks in the system, which allows for the hitless switching of clocks. Bedrosian teaches an alternative method of hitless clock protection switching. There are many other examples of hitless protection switching of clock references in the prior art, therefore the details of the implementation would be a design choice.

***Allowable Subject Matter***

16. Claims 10 - 13 objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.



17. Claims 19 - 23 objected to as being dependent upon rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

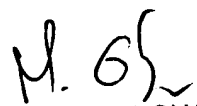
***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Meek whose telephone number is (703) 305-8953. The examiner can normally be reached on 8:00 - 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (703) 306-3034. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JM

  
**MOHAMMAD H. GHAYOUR**  
**PRIMARY EXAMINER**